PATENT ABSTRACTS OF JAPAN

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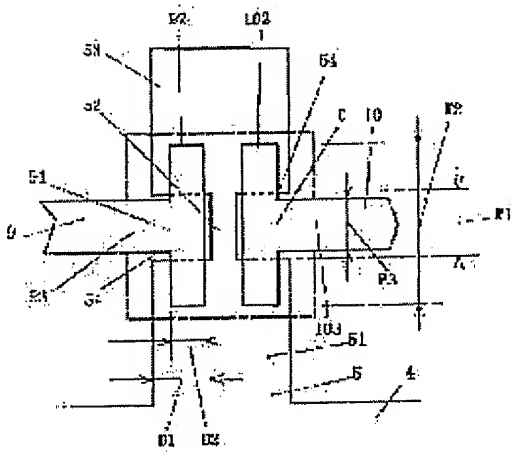
(54) THIN-FILM TRANSISTOR AND ARRAY THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce a parasitic capacity caused by errors in exposure and the like.
SOLUTION: A source electrode 9 and a drain electrode 10 have a horizontally T-shaped part 91 or 101 in a region, where these electrodes 9 and 10 are overlapped horizontally with a semiconductor layer. In a flat gate electrode 5, a base pattern 51 and a top pattern 53 are joined with a narrow joining part 52, and each side groove 54 with a given width is provided on both sides of the joining part 52. In this thin-film transistor, the source and drain electrodes 9 and 10 are formed with the groove 54 in such a way that crosswise polar parts 91 and 102 facing each other are formed on both side of the joining part 52, and lengthwise parts 93 and 103 do not overlap with the gate electrode 5.



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CLAIMS

[Claim(s)]
[Claim 1] The semi-conductor layer which forms a channel field. and the source electrode and drain electrode which intervened and carried out opposite arrangement of this semi-conductor layer. In a thin film transistor equipped with the gate electrode arranged through an insulating layer on said semi-conductor layer or to the bottom so that it may have said source electrode and a drain electrode. and a superficial lap Said

source and a drain electrode equip with and constitute the part into which a flat surface constitutes a T character configuration to the field which laps with said semi-conductor layer and flat-surface target, respectively. Said gate electrode A base pattern and a tip pattern are connected through the connection section of a narrow width, and it constitutes from a flat-surface configuration which formed the slot of predetermined width of face in the both sides of this connection section. Said source and a drain electrode The thin film transistor characterized by having arranged corresponding to said slot so that the bar part of T characters may face mutually on both sides of said connection section. and so that the vertical line part of T characters may not lap with said gate electrode and flat-surface target.
[Claim 2] The semi-conductor layer which forms a channel field, and the source electrode and drain electrode which intervened and carried out opposite arrangement of this semi-conductor layer, In the thin film transistor array which arranged on the substrate the thin film transistor equipped with the gate electrode arranged through an insulating layer on said semi-conductor layer or to the bottom so that it may have said source electrode and a drain electrode. and a superficial lap in the shape of a matrix Said source and a drain electrode equip with and constitute the part into which a flat surface constitutes a T character configuration to the field which laps with said semi-conductor layer and flat-surface target, respectively. Said gate electrode A base pattern and a tip pattern are connected through the connection section of a narrow width. and it constitutes from a flat-surface configuration which formed the slot of predetermined width of face in the both sides of this connection section. Said source and a drain electrode Thin film transistor array characterized by having arranged corresponding to said slot so that the bar part of T characters may face mutually on both sides of said connection section, and so that the vertical line part of T characters may not lap with said gate electrode and flat-surface target.

[Translation done]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a thin film transistor and its array.
[0002]
[Description of the Prior Art] The thin film transistor array which uses for a liquid crystal display etc. connects the semi-conductor layer SC which forms a channel field to the source electrode S which carried out opposite arrangement, and a drain electrode D, as a rough top view is shown in drawing 4 as the thin film transistor, arranges two or more things of the structure equipped with the gate electrode G arranged through an insulating layer on the semi-conductor layer SC or to the bottom so that it may have the source electrode S and the drain electrode D, and a superficial lap, and constitutes them.
[0003] Division exposure which the thin film transistor array used for a liquid crystal display etc. divides one screen into some in the FOTORISO process for carrying out patterning of various kinds of thin films if the flat-surface dimension becomes large-sized, and is exposed is performed in many cases. If division exposure is performed, it is tended to change the area of the part (hatching shows to drawing 4) to which the source electrode D and the drain electrode D lap with the gate electrode G superficially according to the error of the manufacture precision resulting from gap of a mask pattern etc. The parasitic capacitance of a transistor may change with fluctuation of such a lap field of an electrode, and display grace may fall by it. In order to reduce the effect by the parasitic capacitance of a transistor, it is also effective to aim at increase of auxiliary capacity, but if auxiliary capacity is increased, generally it will be easy to cause decline in a numerical aperture.
[0004]
[Problem(s) to be Solved by the Invention] This invention makes it a technical problem to reduce fluctuation of the superficial lap field (parasitic capacitance) of the electrode resulting from an exposure error etc. in a thin film transistor in consideration of the above-mentioned point. Moreover, let it be a technical problem to offer the suitable thin film transistor array for the good liquid crystal display of display grace.
[0005]
[Means for Solving the Problem] The semi-conductor layer in which the thin film transistor of this invention forms a channel field, The source electrode and drain electrode which intervened and carried out opposite arrangement of this semi-conductor layer, In a thin film transistor equipped with the gate electrode arranged through an insulating layer on said semi-conductor layer or to the bottom so that it may have said source electrode and a drain electrode, and a superficial lap Said source and a drain electrode equip with and constitute the part into which a flat surface constitutes a T character configuration to the field which laps with said semi-conductor layer and flat-surface target, respectively. Said gate electrode A base pattern and a tip pattern are connected through the connection section of a narrow width, and it constitutes from a flat-surface configuration which formed the slot of predetermined width of face in the both sides of this connection section. Said source and a drain electrode It is characterized by having arranged corresponding to said slot so that the vertical line part of T characters may not lap with said gate electrode and flat-surface target so that the bar part of T characters may face mutually on both sides of said connection section.
[0006] The semi-conductor layer in which the thin film transistor array of this invention forms a channel field, The source electrode and drain electrode which intervened and carried out opposite arrangement of this semi-conductor layer, In the thin film transistor array which arranged on the substrate the thin film transistor equipped with the gate electrode arranged through an insulating layer on said semi-conductor layer or to the bottom so that it may have said source electrode and a drain electrode, and a superficial lap in the shape of a matrix Said source and a drain electrode equip with and constitute the part into which a flat surface constitutes a T character configuration to the field which laps with said semi-conductor layer and flat-surface target, respectively. Said gate electrode A base pattern and a tip pattern are connected through the connection section of a narrow width. and it constitutes from a flat-surface configuration which formed the slot of predetermined width of face in the both sides of this connection section. Said source and a drain electrode It is characterized by having arranged corresponding to said slot so that the vertical line part of T characters may not lap with said gate electrode and flat-surface target so that the bar part of T characters may face mutually on both sides of said connection section.
[0007]
[Embodiment of the Invention] The example of this invention is explained with reference to a drawing taking the case of the thin film transistor array which arranged the thin film transistor (Thin Film Transistor:TFT) of a reverse stagger mold in the shape of a matrix below. It is the

typical top view in which the rough top view of the thin film transistor array 1 concerning the example of this invention in drawing 1 and drawing 2 show the sectional view of the important section (thin film transistor 2) of drawing 1 , and drawing 3 shows arrangement of the important section (the source electrode of a thin film transistor 2, a drain electrode, gate electrode) of drawing 1 .

[0008] The thin film transistor array 1 is in two or more gate wiring 4 of a longitudinal direction, and a list on the transparence substrates 3, such as alkali free glass. The gate electrode 5 linked to this gate wiring 4 is formed. On said gate electrode 5, the TFT island 7 is formed through the gate insulating layers (SiNx etc) 6. The TFT island 7 is equipped with thin film layers which are connected to the source electrode 9 and the drain electrode 10 which are mentioned later, and form a channel field. such as the a-Si layer 71 as a semi-conductor layer. and the n+a-Si layer 72 for ohmic contacts. The drain electrode 10 is formed in the source wiring 8 of the direction which intersects perpendicularly with the gate wiring 4, the source electrode 9 linked to this, and a list after formation of the TFT island 7. As for wiring 4 and 8, metals, such as Cr, Mo-Ta, and Ta-aluminum. are alternatively used for said electrodes 5 and 9 and 10 lists.

[0009] Top faces, such as the TFT island 7. the source electrode 9, and the drain electrode 10, are covered by protective coats (SiNx etc) 11. After forming in this protective coat 11 the contact hole 12 which results in said drain electrode 10. a thin film transistor 2 is adjoined and the transparent pixel electrodes 13, such as ITO, are formed.

[0010] Said gate electrode 5 has constituted the flat-surface configuration equipped with the base pattern 51 linked to the gate wiring 4, and the tip pattern 53 connected to this base pattern 51 through the connection section 52 of a narrow width, as that superficial pattern is shown in drawing 3 with the source electrode 9 and the drain electrode 10. The predetermined width of face W1 and the slots 54 and 54 of the depth D1 are formed in the both sides of said connection section 52.

[0011] As the source electrode 9 and the drain electrode 10 which opposite arrangement was carried out and were connected to the a-Si layer 71 through the n+a-Si layer 72 are shown in drawing 3 , respectively, the flat surface equips the field which laps with the TFT island 7 (semi-conductor layer) superficially with the part 91,101 which constitutes a T character configuration. And said source electrode 9 and the drain electrode 10 are arranged in the location corresponding to said slot 54 of the bar part 92,102 of the T character configuration 91,101 so that the vertical line part 93,103 of the T character configuration 91,101 may not lap with said gate electrode 5 superficially, while arranging, respectively so that it may face mutually on both sides of the connection section 52 of the gate electrode 5. That is, the die length W2 of the bar part 92,102 of the T character configuration 91,101 is formed so that it may become sufficiently longer than the width of face W1 of a slot 54, the width of face D2 of the bar part 92,102 of the T character configuration 91,101 is short formed a little rather than the depth D1 of a slot 54, and width-of-face W3 of the vertical line part 93,103 of the T character configuration 91,101 is formed so that it may become short a little rather than the width of face W1 of a slot 54.

[0012] Since the slots 54 and 54 of the above pairs were formed in the gate electrode 5 and it has arranged corresponding to slots 54 and 54 by making each flat-surface configuration of the source electrode 9 and the drain electrode 10 into the above T character configurations Even if division exposure etc. originates and gap of the some on precision arises in the upper and lower sides and right and left on the occasion of formation of each electrode, change hardly arises in the superficial lap dimension of the drain electrode 10 and the gate electrode 5 at source electrode 9 list. Since fluctuation of the parasitic capacitance of a thin film transistor 2 is hardly produced in connection with it, either, when this thin film transistor array 1 is included in one substrate of a liquid crystal display and it constitutes a display, generating of the display nonuniformity resulting from parasitic capacitance can be prevented, and the good liquid crystal display of display grace can be offered. Moreover, since the increment in auxiliary capacity is not needed, either, a numerical aperture can be kept high.

[0013] In addition, although the above-mentioned example was explained taking the case of the reverse stagger mold which has arranged the TFT island 7 through gate dielectric film 6 on the gate electrode 5, this invention is applicable also to TFT of the forward stagger mold which arranges a gate electrode through gate dielectric film on a TFT island.

[0014]

[Effect of the Invention] Since change hardly arises in the superficial lap dimension of a drain electrode and a gate electrode at a source list according to this invention as mentioned above even if gap of the some on precision arises in the upper and lower sides and right and left on the occasion of formation of an electrode, fluctuation of the parasitic capacitance of a thin film transistor can be controlled. Consequently. when this thin film transistor array is included in one substrate of a liquid crystal display and it constitutes a display, generating of the display nonuniformity resulting from parasitic capacitance can be prevented, and the good liquid crystal display of display grace can be offered.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the rough top view of the thin film transistor array concerning the example of this invention.

[Drawing 2] It is the sectional view of the important section (thin film transistor) of drawing 1 .

[Drawing 3] It is the rough top view of the important section (thin film transistor) of drawing 1

[Drawing 4] It is the rough top view of the conventional thin film transistor.

[Description of Notations]

1 Thin Film Transistor Array
2 Thin Film Transistor
4 Gate Wiring
5 Gate Electrode
6 Gate Dielectric Film
7 TFT Island
8 Source Wiring
9 Source Electrode
10 Drain Electrode
13 Pixel Electrode

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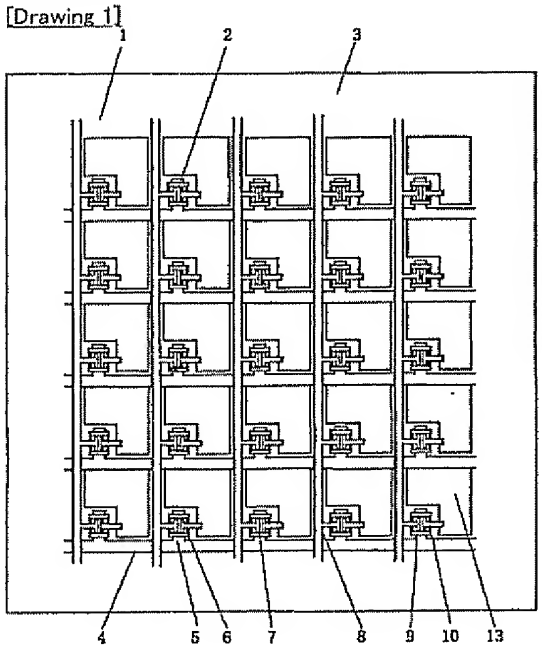
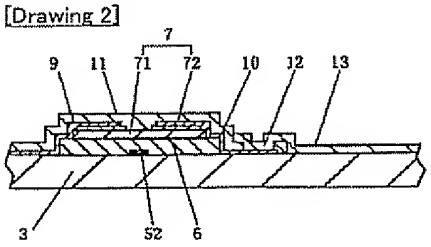
DRAWINGS

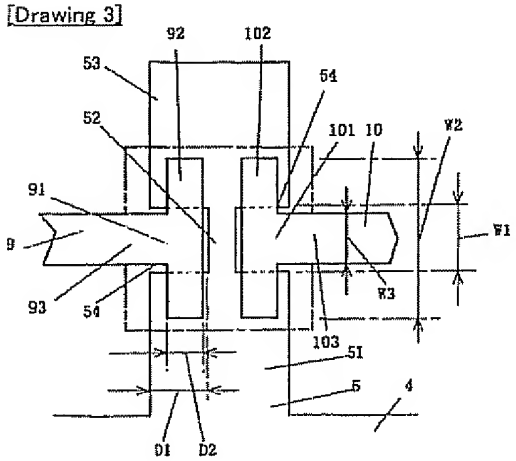
[Drawing 1]



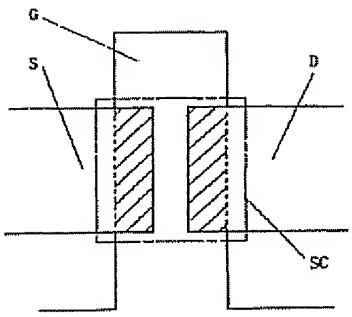
[Drawing 2]



[Drawing 3]



[Drawing 4]



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審査請求　未請求　請求項の数２　ＯＬ　（全４頁）

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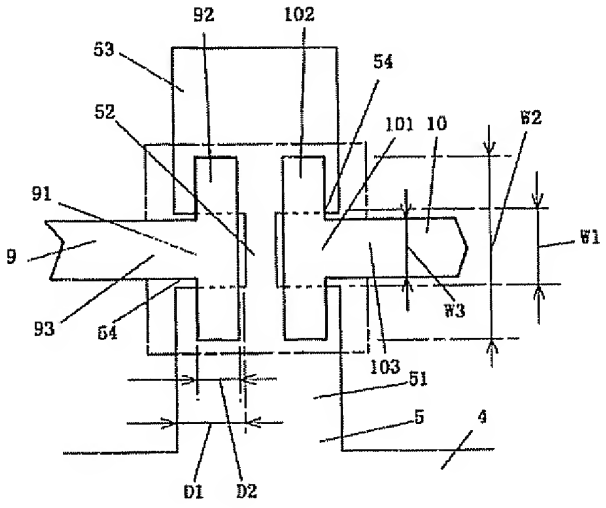
最終頁に続く

(54)【発明の名称】　薄膜トランジスタ及びそのアレイ

(57)【要約】
【課題】　露光誤差等に起因する寄生容量の変動を低減すること。
【解決手段】　ソース電極９及びドレイン電極１０はそれぞれ、半導体層７と平面的に重なる領域に平面がＴ字形状を成す部分９１，１０１を備えている。ゲート電極５は、基部パターン５１と先端パターン５３を細幅の連結部５２を介して接続し、この連結部５２の両側に所定幅の溝部５４を形成した平面形状としている。ソース電極９及びドレイン電極１０は、Ｔ字の横棒部分９２，１０２が連結部５２を挟んで互いに向かい合うように、かつＴ字の縦棒部分９３，１０３がゲート電極５と平面的に重ならないように溝部５４に対応して配置して薄膜トランジスタを構成した。



【特許請求の範囲】

【請求項１】　チャンネル領域を形成する半導体層と、該半導体層を介在して対向配置したソース電極及びドレイン電極と、前記ソース電極及びドレイン電極と平面的な重なりを持つように前記半導体層の上もしくは下に絶縁層を介して配置したゲート電極を備える薄膜トランジスタにおいて、前記ソース及びドレイン電極はそれぞれ、前記半導体層と平面的に重なる領域に平面がＴ字形状を成す部分を備えて構成し、前記ゲート電極は、基部パターンと先端パターンを細幅の連結部を介して接続し、この連結部の両側に所定幅の溝部を形成した平面形状で構成し、前記ソース及びドレイン電極は、Ｔ字の横棒部分が前記連結部を挟んで互いに向かい合うように、かつＴ字の縦棒部分が前記ゲート電極と平面的に重ならないように前記溝部に対応して配置したことを特徴とする薄膜トランジスタ。

【請求項２】　チャンネル領域を形成する半導体層と、該半導体層を介在して対向配置したソース電極及びドレイン電極と、前記ソース電極及びドレイン電極と平面的な重なりを持つように前記半導体層の上もしくは下に絶縁層を介して配置したゲート電極とを備える薄膜トランジスタを基板上にマトリックス状に配列した薄膜トランジスタアレイにおいて、前記ソース及びドレイン電極はそれぞれ、前記半導体層と平面的に重なる領域に平面がＴ字形状を成す部分を備えて構成し、前記ゲート電極は、基部パターンと先端パターンを細幅の連結部を介して接続し、この連結部の両側に所定幅の溝部を形成した平面形状で構成し、前記ソース及びドレイン電極は、Ｔ字の横棒部分が前記連結部を挟んで互いに向かい合うように、かつＴ字の縦棒部分が前記ゲート電極と平面的に重ならないように前記溝部に対応して配置したことを特徴とする薄膜トランジスタアレイ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は薄膜トランジスタ及びそのアレイに関する。

【０００２】

【従来の技術】液晶表示装置等に用いる薄膜トランジスタアレイは、その薄膜トランジスタとして、図４に概略的な平面図を示すように、対向配置したソース電極Ｓ及びドレイン電極Ｄにチャンネル領域を形成する半導体層ＳＣを接続し、ソース電極Ｓ及びドレイン電極Ｄと平面的な重なりを持つように半導体層ＳＣの上もしくは下に絶縁層を介して配置したゲート電極Ｇを備えた構造のものを複数配列して構成している。

【０００３】液晶表示装置等に用いる薄膜トランジスタアレイは、その平面寸法が大型になると、各種の薄膜をパターニングするためのフォトリソ工程において、１つの画面をいくつかに分割して露光する分割露光が行われることが多い。分割露光を行うと、マスクパターンのズレ等に起因する製作精度の誤差によってソース電極Ｄ，ドレイン電極ＤがゲートＧと平面的に重なる部分（図４にハッチングで示す）の面積が変動しやすい。このような電極の重なり領域の変動によって、トランジスタの寄生容量が変化し、それによって表示品位が低下することがある。トランジスタの寄生容量による影響を低減するためには、補助容量の増大を図ることも有効であるが、補助容量を増大させると一般に開口率の低下を招きやすい。

【０００４】

【発明が解決しようとする課題】本発明は上記の点を考慮し、薄膜トランジスタにおいて、露光誤差等に起因する電極の平面的な重なり領域（寄生容量）の変動を低減することを課題とする。また、表示品位の良好な液晶表示装置に好適な薄膜トランジスタアレイを提供することを課題とする。

【０００５】

【課題を解決するための手段】本発明の薄膜トランジスタは、チャンネル領域を形成する半導体層と、該半導体層を介在して対向配置したソース電極及びドレイン電極と、前記ソース電極及びドレイン電極と平面的な重なりを持つように前記半導体層の上もしくは下に絶縁層を介して配置したゲート電極を備える薄膜トランジスタにおいて、前記ソース及びドレイン電極はそれぞれ、前記半導体層と平面的に重なる領域に平面がＴ字形状を成す部分を備えて構成し、前記ゲート電極は、基部パターンと先端パターンを細幅の連結部を介して接続し、この連結部の両側に所定幅の溝部を形成した平面形状で構成し、前記ソース及びドレイン電極は、Ｔ字の横棒部分が前記連結部を挟んで互いに向かい合うように、かつＴ字の縦棒部分が前記ゲート電極と平面的に重ならないように前記溝部に対応して配置したことを特徴とする。

【０００６】本発明の薄膜トランジスタアレイは、チャンネル領域を形成する半導体層と、該半導体層を介在して対向配置したソース電極及びドレイン電極と、前記ソース電極及びドレイン電極と平面的な重なりを持つように前記半導体層の上もしくは下に絶縁層を介して配置したゲート電極とを備える薄膜トランジスタを基板上にマトリックス状に配列した薄膜トランジスタアレイにおいて、前記ソース及びドレイン電極はそれぞれ、前記半導体層と平面的に重なる領域に平面がＴ字形状を成す部分を備えて構成し、前記ゲート電極は、基部パターンと先端パターンを細幅の連結部を介して接続し、この連結部の両側に所定幅の溝部を形成した平面形状で構成し、前記ソース及びドレイン電極は、Ｔ字の横棒部分が前記連結部を挟んで互いに向かい合うように、かつＴ字の縦棒部分が前記ゲート電極と平面的に重ならないように前記溝部に対応して配置したことを特徴とする。

【０００７】

【発明の実施の形態】以下本発明の実施例を逆スタガ型

の薄膜トランジスタ（Thin Film Transistor：ＴＦＴ）をマトリックス状に配列した薄膜トランジスタアレイを例にとって図面を参照して説明する。図１は本発明の実施例に係わる薄膜トランジスタアレイ１の概略的な平面図、図２は図１の要部（薄膜トランジスタ２）の断面図、図３は図１の要部（薄膜トランジスタ２のソース電極、ドレイン電極、ゲート電極）の配置を示す模式的な平面図である。

【０００８】薄膜トランジスタアレイ１は、無アルカリガラスなどの透明基板３の上に、左右方向の複数のゲート配線４、並びに　このゲート配線４に接続したゲート電極５を形成している。前記ゲート電極５の上には、ゲート絶縁層（ＳｉＮｘ等）６を介してＴＦＴアイランド７を形成している。ＴＦＴアイランド７は、後述するソース電極９やドレイン電極１０に接続されてチャンネル領域を形成する半導体層としてのａ－Ｓｉ層７１やオーミックコンタクト用のｎ⁺ａ－Ｓｉ層７２などの薄膜層を備えている。ＴＦＴアイランド７の形成後、ゲート配線４と直交する方向のソース配線８、これに接続したソース電極９，並びにドレイン電極１０が形成される。前記電極５，９，１０並びに配線４，８は、Ｃｒ，Ｍｏ－Ｔａ，Ｔａ－Ａｌなどの金属が選択的に使用される。

【０００９】ＴＦＴアイランド７、ソース電極９、ドレイン電極１０などの上面は、保護膜（ＳｉＮｘ等）１１によって覆っている。この保護膜１１に前記ドレイン電極１０に至るコンタクトホール１２を形成した後、ＩＴＯ等の透明な画素電極１３を薄膜トランジスタ２に隣接して形成している。

【００１０】前記ゲート電極５は、図３にその平面的なパターンをソース電極９及びドレイン電極１０とともに示すように、ゲート配線４に接続した基部パターン５１と、この基部パターン５１に細幅の連結部５２を介して接続した先端パターン５３を備えた平面形状を成している。前記連結部５２の両側には、所定の幅Ｗ１と深さＤ１の溝部５４，５４が形成されている。

【００１１】対向配置されてｎ⁺ａ－Ｓｉ層７２を介してａ－Ｓｉ層７１に接続されたソース電極９とドレイン電極１０はそれぞれ、図３に示すように、ＴＦＴアイランド７（半導体層）と平面的に重なる領域に、平面がＴ字形状を成す部分９１，１０１を備えている。そして、前記ソース電極９及びドレイン電極１０は、Ｔ字形状９１，１０１の横棒部分９２，１０２のそれぞれが、ゲート電極５の連結部５２を挟んで互いに向かい合うように配置しているとともに、Ｔ字形状９１，１０１の縦棒部分９３，１０３が前記ゲート電極５と平面的に重ならないように前記溝部５４に対応した位置に配置している。すなわち、Ｔ字形状９１，１０１の横棒部分９２，１０２の長さＷ２を溝５４の幅Ｗ１よりも十分長くなるように形成し、Ｔ字形状９１，１０１の横棒部分９２，１０２の幅Ｄ２を溝５４の深さＤ１よりも若干短く形成し、Ｔ字形状９１，１０１の縦棒部分９３，１０３の幅Ｗ３を溝５４の幅Ｗ１よりも若干短くなるように形成している。

【００１２】ゲート電極５に上記のような一対の溝部５４，５４を形成し、ソース電極９，ドレイン電極１０の各々の平面形状を上記のようなＴ字形状として溝部５４，５４と対応して配置したので、各電極の形成に際して、分割露光など起因して上下、左右に精度上の若干のズレが生じたとしても、ソース電極９並びにドレイン電極１０とゲート電極５の平面的な重なり寸法に変化が殆ど生じない。それにともない、薄膜トランジスタ２の寄生容量の変動も殆ど生じないので、この薄膜トランジスタアレイ１を液晶表示装置の一方の基板に組み込んで表示装置を構成する場合、寄生容量に起因する表示ムラの発生を防止して表示品位の良い液晶表示装置を提供することができる。また、補助容量の増加も必要としないので、開口率を高く保つことができる。

【００１３】尚、上記実施例は、ゲート電極５の上にゲート絶縁膜６を介してＴＦＴアイランド７を配置した逆スタガ型を例にとって説明したが、本発明は、ＴＦＴアイランドの上にゲート絶縁膜を介してゲート電極を配置する正スタガ型のＴＦＴにも適用することができる。

【００１４】

【発明の効果】以上のように本発明によれば、電極の形成に際して、上下、左右に精度上の若干のズレが生じたとしても、ソース並びにドレイン電極とゲート電極の平面的な重なり寸法に変化が殆ど生じないので、薄膜トランジスタの寄生容量の変動を抑制することができる。その結果、この薄膜トランジスタアレイを液晶表示装置の一方の基板に組み込んで表示装置を構成する場合、寄生容量に起因する表示ムラの発生を防止して表示品位の良い液晶表示装置を提供することができる。

【図面の簡単な説明】

【図１】本発明の実施例に係わる薄膜トランジスタアレイの概略的な平面図である。

【図２】図１の要部（薄膜トランジスタ）の断面図である。

【図３】図１の要部（薄膜トランジスタ）の概略的な平面図である。

【図４】従来の薄膜トランジスタの概略的な平面図である。

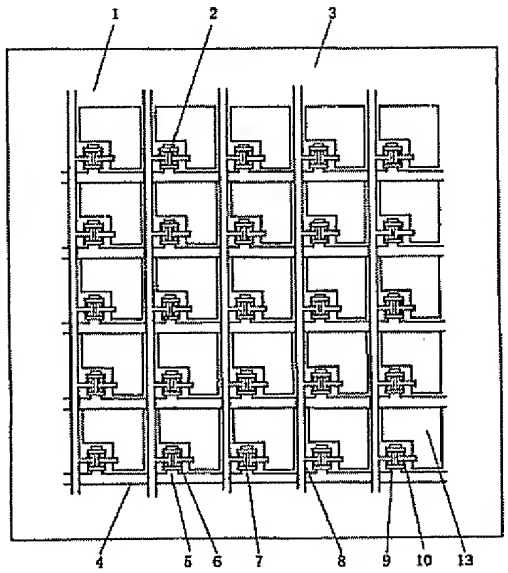
【符号の説明】

１　薄膜トランジスタアレイ
２　薄膜トランジスタ
４　ゲート配線
５　ゲート電極
６　ゲート絶縁膜
７　ＴＦＴアイランド
８　ソース配線
９　ソース電極

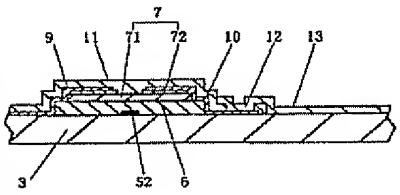
１０　ドレイン電極

１３　画素電極

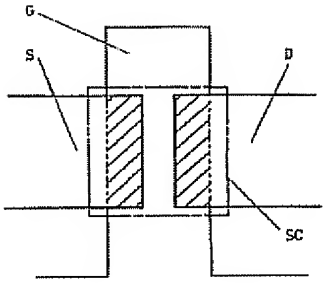
【図１】



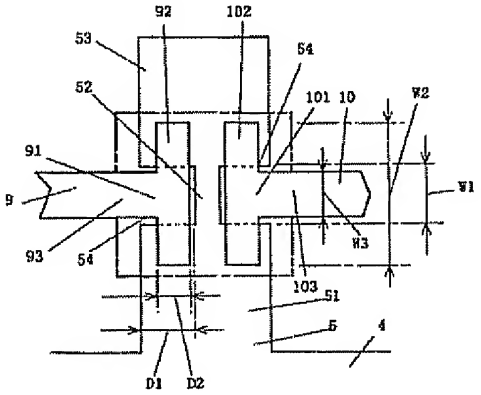
【図２】



【図４】



【図３】



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